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ECE 4203

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**PROJECT 2: SPICE Simulations for Logical Effort**

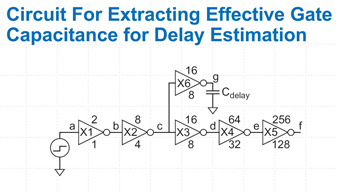
**Logical Effort**

1. Find the effective gate capacitance (per µm transistor width) for the process by using procedure in “Weste and Harris”, section 8.4.3. For this simulation use inverters as shown in the schematic below.

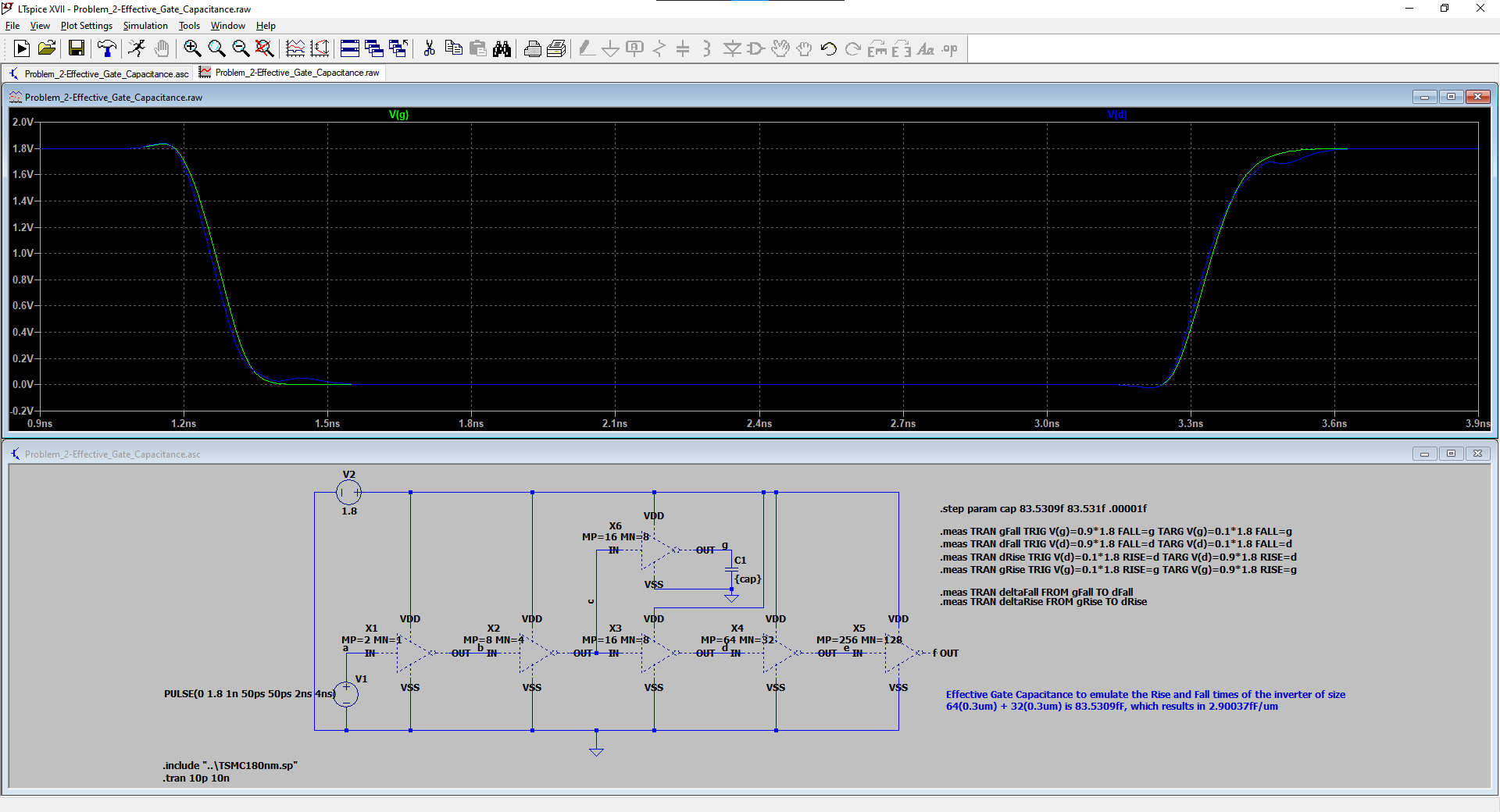
Hints:

* 1. For this simulation, make sure to set the transistor parameters related to output diffusion area to zero (i.e. set AD, AS, PD, PS to zero for both NMOS and PMOS). If you do not do this, you will not be able to isolate just the gate capacitance.
  2. Once you’ve equalized the delays to nodes “d” and “g”, remember to divide by gate width of your load to get fF/µm of transistor width (note that is the not capacitance per unit area, so you’ll have to

normalize for gate length.



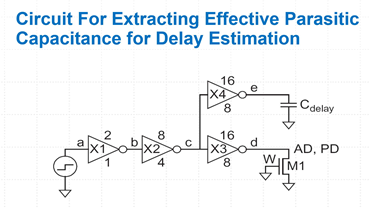
**My effective gate capacitance is 81.5309 fF / ((64(300nm) +32(300nm)) = 2.90037 fF/µm**



1. Find the effective parasitic capacitance of the transistor drains (per µm transistor width) for the process. You will have to do a separate simulation for PMOS. For PMOS the schematic uses a PMOS with its Gate and Source connected to VDD. Use inverters for this simulation.

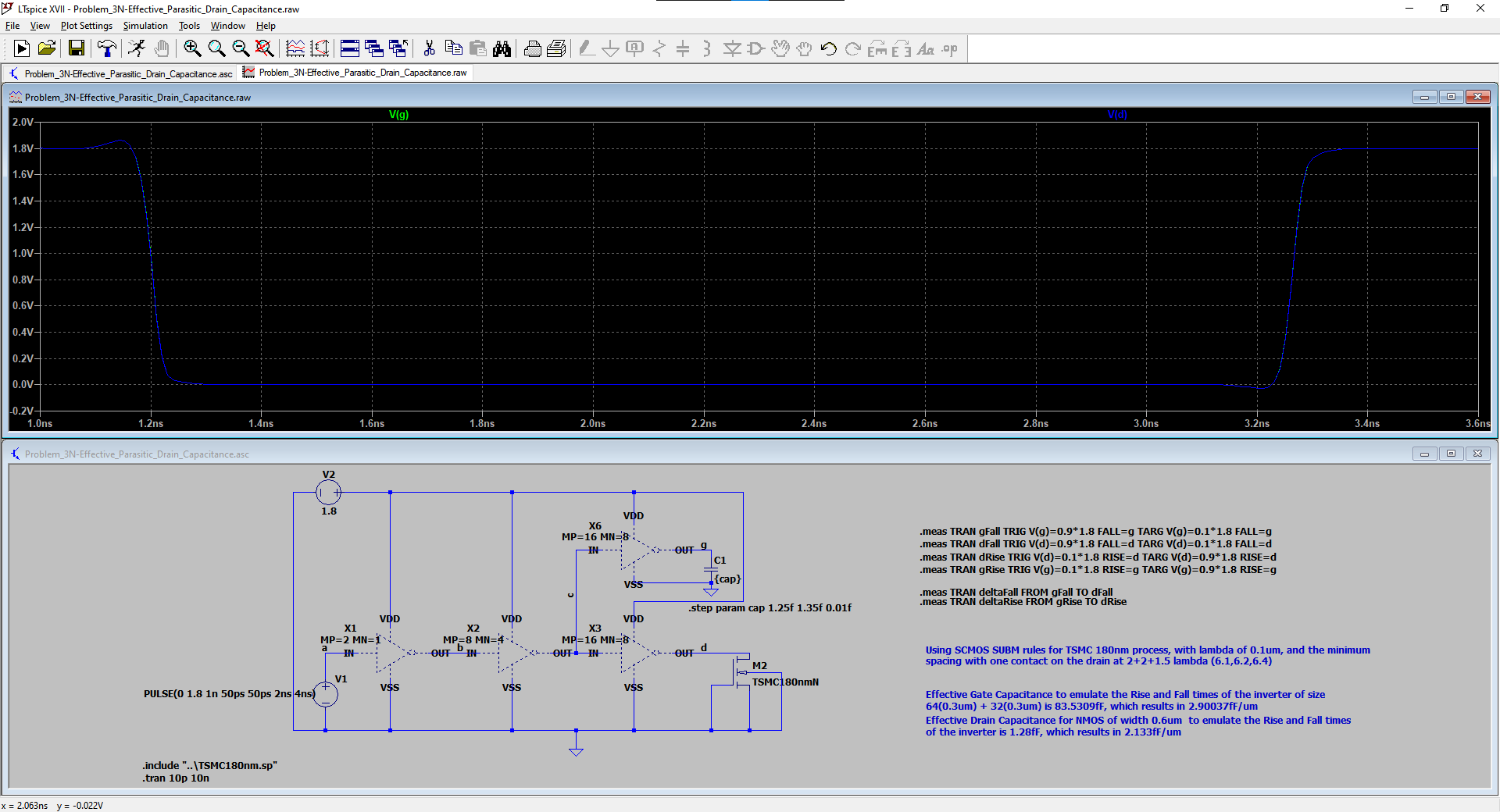
Hints:

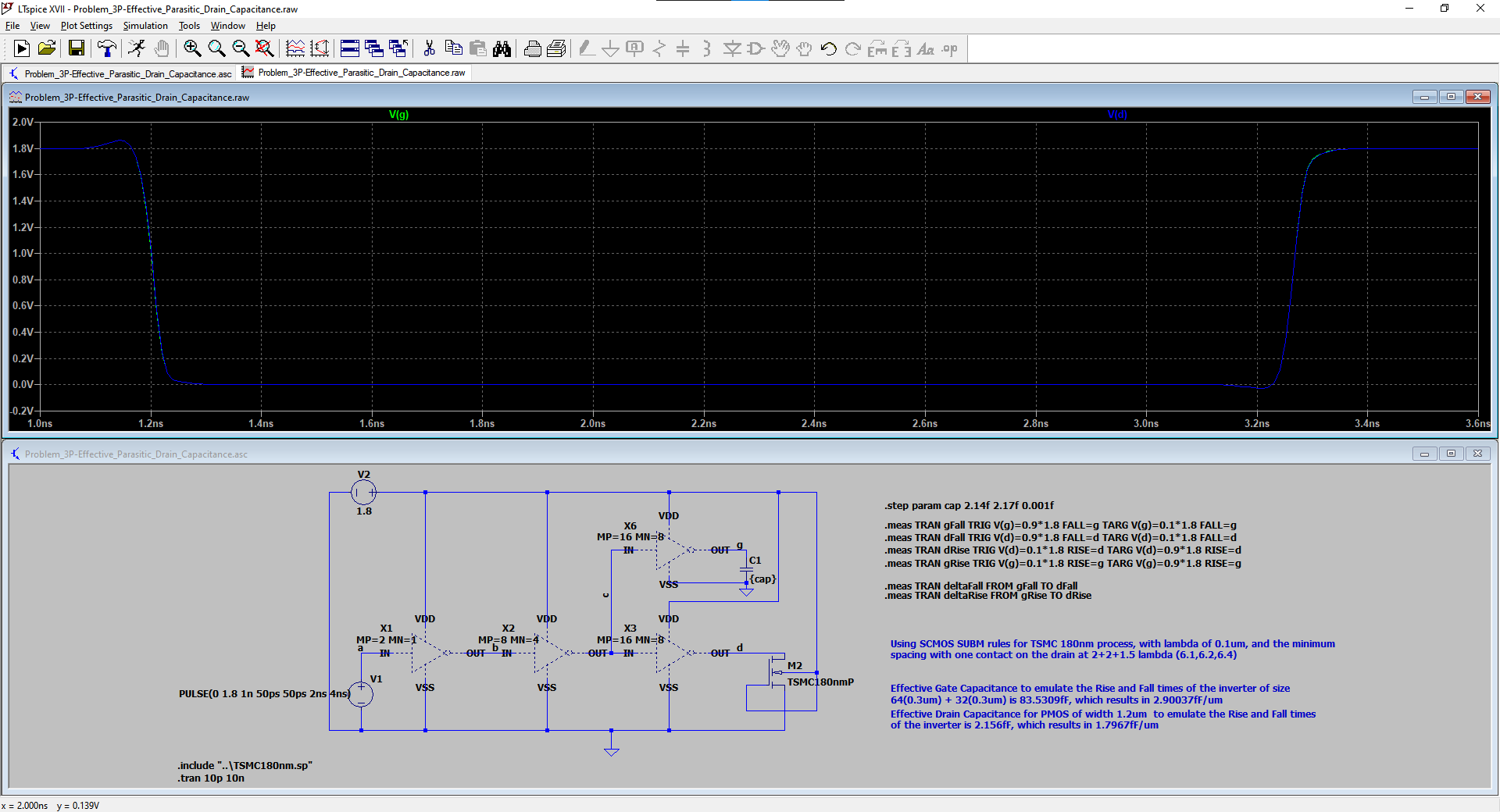
* 1. For this simulation, make sure to set the transistor parameters related to output diffusion area to the appropriate value (i.e. calculate AD, AS, PD, PS to zero for both NMOS and PMOS). If you do not, you will not get the appropriate diffusion capacitance. Watch you units carefully here – you can easily end up with orders of magnitude higher capacitance).
  2. Once you have equalized the delays to nodes “d” and “g”, remember to divide by gate width of your load to get fF/μm of transistor width.



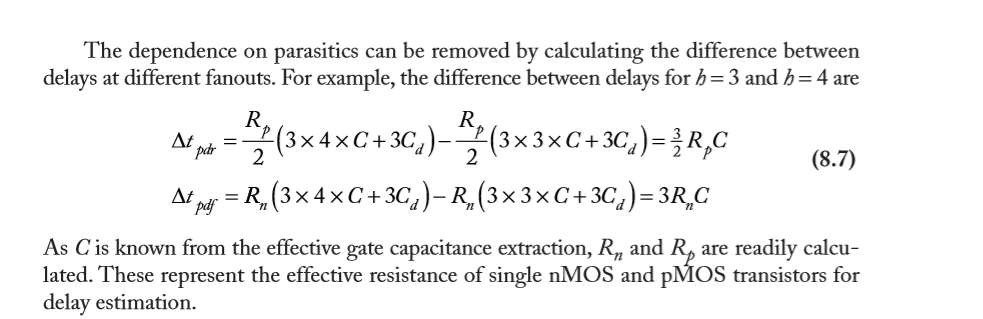
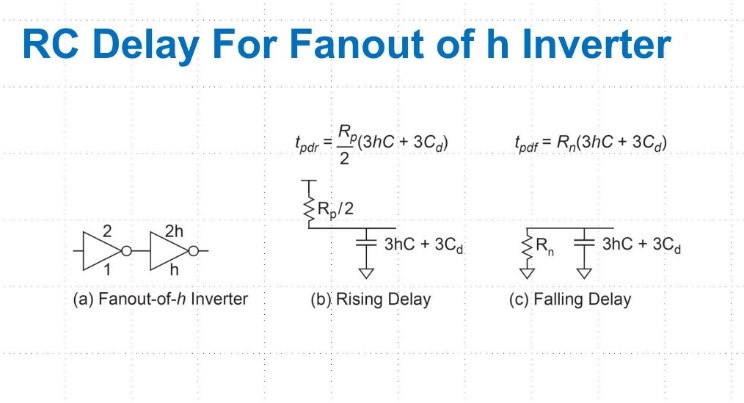
|  |  |  |
| --- | --- | --- |
| **λ = .1\*10-6** | **NMOS 400nmLx600nmW** | **PMOS 800nmLx1200nmW** |
| **Area of Drain (AD)** | 600nm\*5.5 λ = 330 x 10-15 | 1200nm\*5.5 λ = 660 x 10-15 |
| **Perimeter of Drain (PD)** | 2(600nm) + 2(5.5 λ) = 2300 x 10-9 | 2(1200nm) + 2(5.5 λ) = 3500 x 10-9 |

|  |  |  |
| --- | --- | --- |
| **Transistor** | **Effective Parasitic Drain Capacitance** | **Parasitic Drain Capacitance (Normalized)** |
| PMOS | 2.156 fF | 2.156 fF / 1.200 µm= 1.7967 fF/µm |
| NMOS | 1.28 fF | 1.28 fF / 0.600 µm = 2.133 fF/µm |





1. Calculate the Effective resistance of the process:



Excerpt from "Weste and Harris", section 8.4.5

**Measurement: pdr**

**step pdr FROM TO**

**H=3 6.3034e-011 3.075e-009 3.13803e-009**

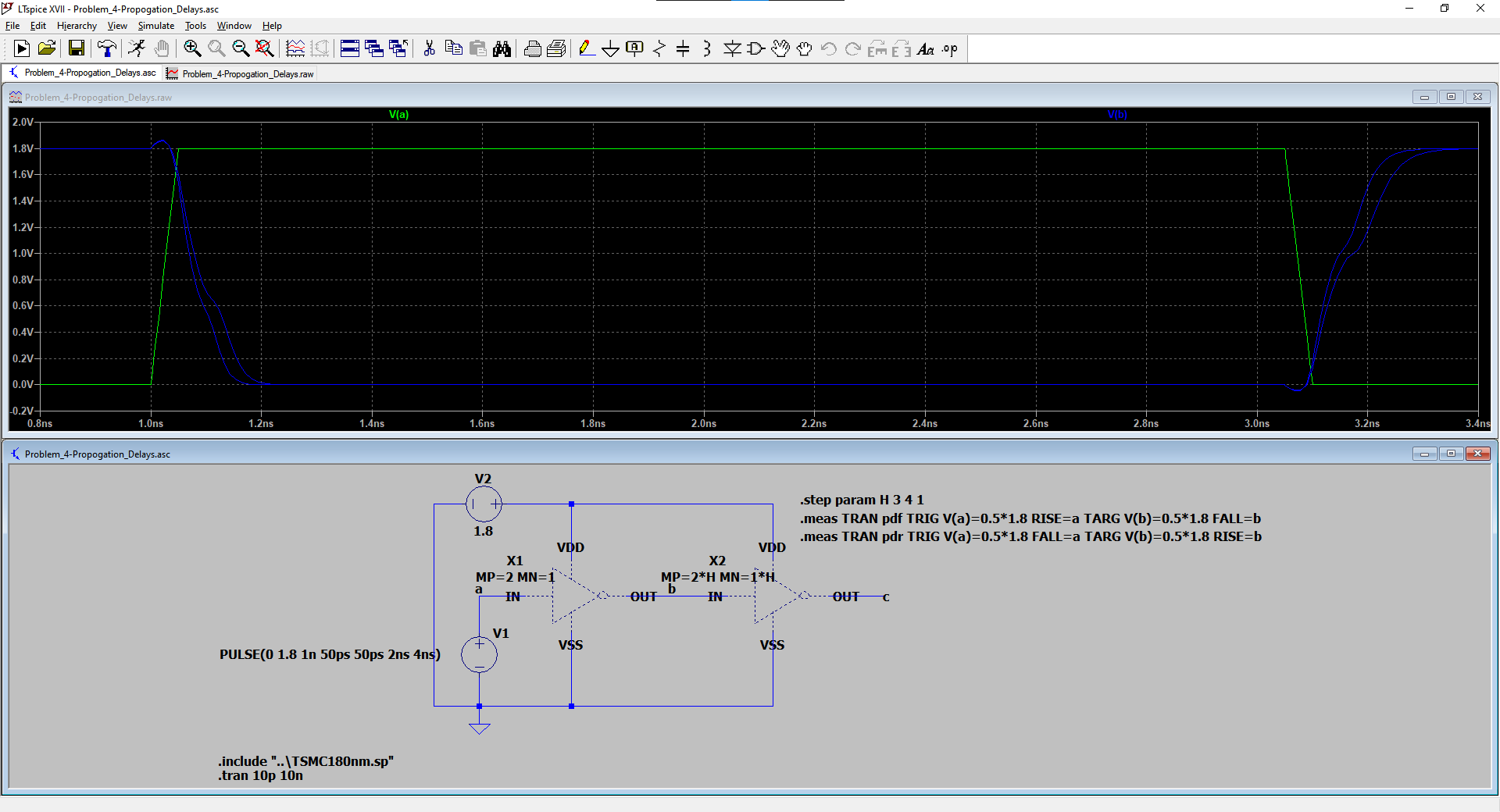
**H=4 7.77734e-011 3.075e-009 3.15277e-009**

**Measurement: pdf**

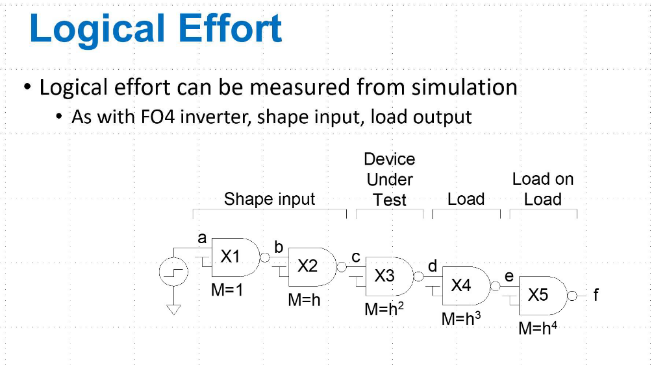
**step pdf FROM TO**

**H=3 4.93458e-011 1.025e-009 1.07435e-009**

**H=4 5.96848e-011 1.025e-009 1.08468e-009**

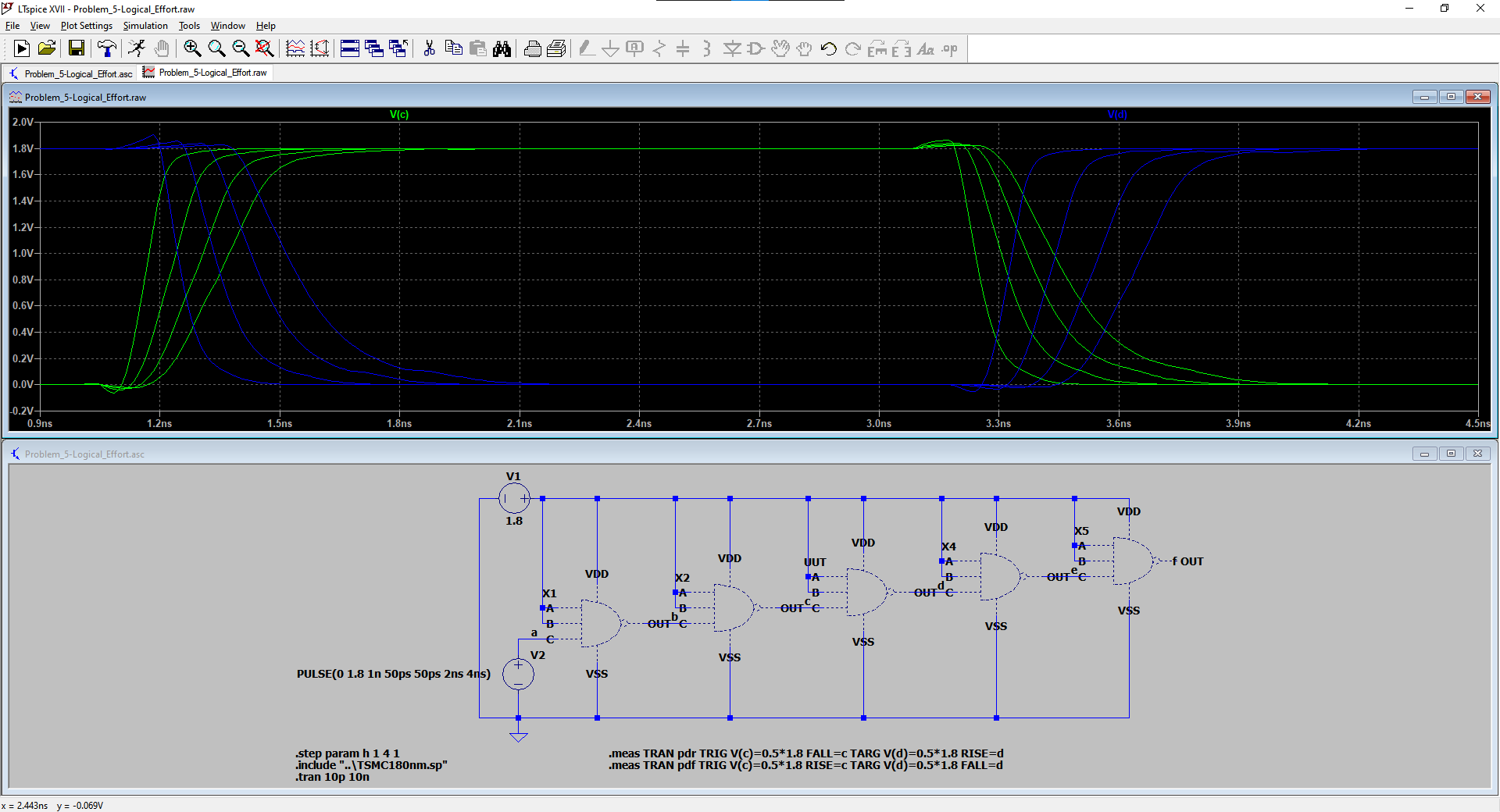


1. Logical effort simulation
2. **Simulate** the logical effort **of the circuit assigned to you in Project 1**.
3. Use the methodology in Section 8.5.3 of Weste and Harris (figure replicated below for your reference).
4. Plot the logical effort for your circuit for h=1, 2, 3, and 4





**Using the graph above and the trendline equation, the y-intercept, at 47.532ps, is the parasitic delay, which went normalized by τ = 15, results in 3.1688 parasitic delay for NAND3 and the slope of the line, 34.073, is the logical effort, which when normalized by τ = 15, results in 2.2715 logical effort for NAND3**

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1. Logical effort calculation
2. **Calculate** the logical effort **of the circuit assigned to you in Project 1**.
3. Plot the logical effort for your circuit for h=1, 2, 3, and 4 using the values for gate capacitance, parasitic capacitance, and equivalent resistance that you found in problems steps 2, 3, and 5.



**Results:**

1. **Write down your simulated values for RN, RP, Cgn, Cgp, Cdn, Cdp from 2,3 and 4 above.**
2. **Use Microsoft Excel to merge the two plots created in 5c and 6b**
3. **Turn in a printout with both. Make sure to include your name.**

**The graph below is an example of what this should look like (the example is for a minimum sized inverter).**





**Final Values:**

|  |  |  |
| --- | --- | --- |
| **Property** | **Equivalent Value** | **Per µm** |
| **Rn** |  |  |
| **Rp** |  |  |
| **Cgn** | 83.5309fF | 2.90037 fF/µm |
| **Cgp** | 83.5309fF | 2.90037 fF/µm |
| **Cdn** | 1.28 fF | 2.133 fF/µm |
| **Cdp** | 2.156 fF | 1.7967 fF/µm |